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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/469,960	12/21/1999	MARK L. SKARPNESS	10559/095001	5596

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EXAMINER	
BLAIR, DOUGLAS B	

ART UNIT	PAPER NUMBER
2142	13

DATE MAILED: 10/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/469,960	SKARPNESS, MARK L.	
	Examiner	Art Unit	
	Douglas B Blair	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-10 and 13-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-10 and 13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Claims 3-10 and 13-24 are currently pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 3-5, 7-10, 13-20, 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 6,088,734 to Marin et al..

4. As to claim 3, Marin teaches a computer system comprising: a host processor (col. 6, lines 7-14); a peripheral device configured to transfer data form a network to the host processor over an attachment bus inside the computer system using at least first and second types of data transfers (col. 6, lines 52-67 and col. 7, lines 1-37), comprising: a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer (col. 6, lines 52-67 and col. 7, lines 1-8); a first queue connected to receive the first class of data form the classifying circuit (col. 7, lines 9-37); a second queue connected to receive the second class of data from the classifying circuit (col. 7, lines 9-37); and a control circuit configured to place data format he first queue onto the bus at a higher priority than data format he second queue is placed onto the bus (col. 7, lines 9-37); where

the bus is configured to receive data during time cycles of predetermined length (col. 10, lines 11-35); where the control circuit is configured to place at least a minimum amount of data from the first queue onto the bus during each time cycle (col. 10, lines 21-54); where the control circuit is configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied by the first class data (col. 11, lines 14-38).

5. As to claim 4, Marin teaches the system of claim 3, where the peripheral device includes a network interface component connected to receive the data form a computer network (col. 7, lines 9-37).

6. As to claim 5, Marin teaches the system of claim 3, wherein the data includes packetized voice data (col. 9, lines 34-55).

7. As to claim 7, Marin teaches the system of claim 3, where the peripheral device is configured to deliver the data packets of predetermined length (col. 10, lines 21-35, ATM cells have a fixed length.).

8. As to claim 8, Marin teaches the system of claim 7, where the classifying circuit is configured to place each of the packets into one of the queues (col. 7, lines 9-37).

9. As to claim 9, Marin teaches a computer system comprising: a host processor (col. 6, lines 7-14); a peripheral device configured to transfer data form a network to the host processor over an attachment bus inside the computer system using at least first and second types of data transfers (col. 6, lines 52-67 and col. 7, lines 1-37), comprising: a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer (col. 6, lines 52-67 and col. 7, lines 1-8); a first queue connected to receive the first class of data form the classifying circuit (col. 7, lines 9-37); a

second queue connected to receive the second class of data from the classifying circuit (col. 7, lines 9-37); and a control circuit configured to place data format he first queue onto the bus at a higher priority than data format he second queue is placed onto the bus (col. 7, lines 9-37); where the bus is configured to receive data during time cycles of predetermined length (col. 10, lines 11-35); where the control circuit is configured to place at least a minimum amount of data from the first queue onto the bus during each time cycle (col. 10, lines 21-54); where a portion of each packet indicates a virtual channel associated with the packet, and where the classifying circuit includes a storage device that stores information indicating each of the virtual channels that is associated with at least one of the classes (col. 6, lines 25-44).

10. As to claim 10, Marin teaches the system of claim 9, where the classifying circuit includes a selection element configured to compare, for each packet the information in the storage device to the data in the portion of the packet that indicates a virtual channel and select a corresponding one of the queues to receive the packet (col. 6, lines 52-67 and col. 7, lines 1-8).

11. As to claims 13-17, they feature the same limitations as claims 3-8 and are rejected for the same reasons as claims 3-8.

12. As to claims 18 and 19, they feature the same limitations as claims 9 and 10 and are rejected for the same reasons as claims 9 and 10.

13. As to claim 20, Marin teaches the system of claim 9, where the classifying circuit comprises a buffer adapted to buffer a received packet, a shift register adapted to store a portion of the received packet, and the storage device is a content addressable memory device adapted to store information indicating each of the virtual channels that is associated with at least one of the classes (col. 7, lines 26-52).

14. As to claim 22, Marin teaches the system of claim 3, wherein the bus uses an Asynchronous Transfer Mode (col. 6, lines 45-51).

15. As to claim 23, it corresponds to the peripheral described in claim 3 and is rejected for the same reasons as the peripheral in claim 3.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 6, 21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 6,088,734 to Marin et al. in view of U.S. Patent Number 6,470,410 to Gulick et al..

As to claim 6, Marin teaches a computer system comprising: a host processor (col. 6, lines 7-14); a peripheral device configured to transfer data form a network to the host processor over an attachment bus inside the computer system using at least first and second types of data transfers (col. 6, lines 52-67 and col. 7, lines 1-37), comprising: a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer (col. 6, lines 52-67 and col. 7, lines 1-8); a first queue connected to receive the first class of data form the classifying circuit (col. 7, lines 9-37); a second queue connected to receive the second class of data from the classifying circuit (col. 7, lines 9-37); and a control circuit configured to place data format he first queue onto the bus at a

higher priority than data format he second queue is placed onto the bus (col. 7, lines 9-37); and the first type of transfer associated with the first class of data is an isochronous transfer, and the second type of transfer is associated with the second class of data is a bulk transfer (col. 10, lines 21-54); however Marin does not explicitly teach the use of USB bus.

Gulick teaches the use of USB in a computer communication system (col. 24, lines 30-63).

It would have been obvious to one of ordinary skill in the Computer Networking art at the time of the invention to combine the teachings of Marin regarding priority queueing with the teachings of Gulick regarding the use of USB in a computer communication system because USB is a common bus architecture (Gulick, col. 24, lines 30-63).

18. As to claim 21, Marin teaches the system of claim 3; however Marin does not explicitly teach the use of a PCI bus.

Gulick teaches the use of a PCI bus (col. 24, lines 30-63).

It would have been obvious to one of ordinary skill in the Computer Networking art at the time of the invention to combine the teachings of Marin regarding priority queueing with the teachings of Gulick regarding the use of a PCI bus in a computer communication system because a PCI bus is a common bus architecture (Gulick, col. 24, lines 30-63).

19. As to claim 24, it corresponds to the peripheral described in claim 6 and is rejected for the same reasons as the peripheral in claim 6.

Response to Arguments

20. Applicant's arguments with respect to claims 3-10 and 13-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas B Blair whose telephone number is 703-305-5267. The examiner can normally be reached on 8:30am-5pm Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on 703-308-5221. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3800.

Douglas Blair
October 1, 2003
DBB

DAVID WILEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100